WHAT IS CLAIMED IS:

1	1. A method of making an integrated circuit in a semiconductor substrate
2	the method comprising:
3	forming at least two isolation regions in the semiconductor substrate;
4	forming a well between the two isolation regions, the well defining a body
5	region;
6	forming a first oxide layer above a first portion of the body region;
7	forming a first dielectric layer above the first oxide layer;
8	forming a first polysilicon layer above said first dielectric layer, said first
9	polysilicon layer forming a control gate of a non-volatile device;
10	forming a second dielectric layer above the first polysilicon layer;
11	forming a first spacer above the body region and adjacent said first polysilicon
12	layer;
13	forming a second oxide layer above a second portion of the body region not
14	covered by said first spacer;
15	forming a second polysilicon layer over the second oxide layer, the first spaces
16	and a portion of the second dielectric layer; said second polysilicon layer forming a guiding
17	gate of the non-volatile device and a gate of an MOS transistor;
18	delivering first implants to the body region to form lightly doped areas in the
19	body region;
20	delivering second implants to the defined source and drain regions;
21	forming a second spacer above the body region to define regions receiving
22	lightly dopes implants and to define a conducting region of a capacitor of the non-volatile
23	cell.
1	2. The method of claim 1 forther commissing.
1	2. The method of claim 1 further comprising:
2	forming a salicide layer over the portions of the lightly doped areas in the
3	body region that form polysilicon landing pads.
1	3. The method of claim 2 further comprising:
2	forming a metal layer over the salicide layer to form a bitline and a terminal
3	adapted to receive a supply voltage.

1 4. The method of claim 3 wherein a doping concentration of the first 2 implants delivered to one of the source and drain regions of the non-volatile device is greater 3 than a doping concentration of the first implants delivered to the other one of the source and 4 drain regions of the non-volatile device. 1 5. The method of claim 4 wherein said first dielectric layer further 2 includes an oxide layer and a nitride layer. 6. 1 The method of claim 5 wherein said second dielectric layer further 2 includes an oxide layer and a nitride layer. 1 7. The method of claim 6 wherein said well is a p-well. 1 8. The method of claim 7 further comprising: 2 forming an n-well below the p-well. 9. 1 The method of claim 8 wherein said n-well is formed using at least one 2 implant step. 1 10. The method of claim 9 wherein at least two implant steps are used to 2 form the n-well using a same mask. 1 11. The method of claim 10 wherein said second oxide layer has a 2 thickness greater than the thickness of the first oxide layer.